REMARKS

The Final Office Action dated December 11, 2007, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-17 are currently pending in the application, of which claims 1, 8-10, and 16-17 are independent claims. In view of the following Remarks, Applicant respectfully requests reconsideration and timely withdrawal of the pending rejections for the reasons discussed below.

Claim Rejections under 35 U.S.C. §102(b)

The Office Action rejected claims 1-17 under 35 U.S.C. §102(b) as being allegedly anticipated by Rusu, *et al.* (U.S. Patent No. 6,137,807) ("Rusu"). The Office Action alleged that Rusu discloses or suggests every claim feature recited in claims 1-17. Applicant respectfully submits that the claims recite subject matter that is neither disclosed nor suggested in Rusu.

Claim 1, upon which claims 2-7 are dependent, recites a method. The method includes receiving a packet, determining an address of a free entry in a queue, placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and placing packet data of the packet in a free entry of a first data structure. There is one-to-one mapping between the queue and the first data structure.

Claim 8 recites a transmit queue system. The transmit queue system includes means for receiving a packet, means for determining an address of a free entry in a queue,

means for placing the determined address in an entry of a prior-determined address in the queue to form a linking list, and means for placing packet data of the packet in a free entry of a first data structure. The transmit queue system also includes one-to-one mapping between the queue and the first data structure.

Claim 9 recites a transmit queue system. The transmit queue system includes a first data structure capable of holding a plurality of packet data, a queue capable of holding a linking list of addresses, a packet receiving engine capable of receiving a packet, a free entry engine coupled to the packet receiving engine and capable of determining an address of a free entry in the queue, a transmit queue engine, and a packet buffer engine. The addresses have a one-to-one mapping with addresses in the first data structure. The transmit queue engine is coupled to the queue, the packet receiving engine, and the free entry engine and is capable of placing the determined address in an entry of a prior-determined address in the queue to form a linking list. The packet buffer engine is coupled to the first data structure, the packet receiving engine, and the free entry engine and is capable of placing packet data of the packet in a free entry of the first data structure.

Claim 10, upon which claims 11-15 are dependent, recites a method of receiving an address in queue, reading packets from an entry from a first data structure with the same address as the received address, the queue, and the first data structure having one-to-one mapping, transmitting the packet data to a network node associated with the

queue, reading a next address in the queue from the received address in the queue, and using the next address to repeat the reading packet data and the transmitting.

Claim 16 recites a transmit queue system. The transmit queue system includes means for receiving an address in a queue, means for reading packet data from an entry from a first data structure with the same address as the received address, means for transmitting the packet data to a network node associated with the queue, means for reading a next address in the queue from the received address in the queue, and means for using the next address to rerun the means for reading packet data and the means for transmitting. The queue and the first data structure have one-to-one mapping.

Claim 17 recites a transmit queue system. The transmit queue system includes a first data structure holding a plurality of packet data, a queue holding a linking list of addresses, and a packet transmit engine. The addresses have a one-to-one mapping with addresses in the first data structure. The packet transmit engine is coupled to the first data structure and the queue. The packet transmit engine is capable of receiving an address in the queue, reading packet data from an entry from the first data structure with the same address as the received address, transmitting the packet data to a network node associated with the queue, reading a next address in the queue from the received address in the queue, and using the next address to repeat the reading packet data and the transmitting.

As will be discussed below, Rusu fails to disclose or suggest every feature recited in claims 1-17, and therefore fails to provide the features discussed above.

Rusu is directed to communication switches and data storage systems for use therewith. Rusu is also directed to a multiple queue bank balanced queue control system architecture. An input processor recognizes and accepts a wide variety of protocols and formats. Queue management stores uniform cells in a dual balanced bank memory system, which provides for utilizing an available bank of memory when the other bank of memory is in use, and otherwise balancing the use of the banks of memory, thereby maintaining equal free lists. Queue management apparatus and logic also ascertains and appends routing data to the stored data and transmits the data according to its priority (Abstract; col. 1, lines 30-52).

Applicant respectfully submits that Rusu fails to disclose or suggest every claim feature recited in claim 1, and similarly recited in claims 8, 9, 10, 16, and 17. Specifically, Rusu fails to disclose or suggest, at least, "placing the determined address in an entry of a prior-determined address in the queue to form a linking list" (emphasis added).

Rather, Rusu discloses a queue number, which is a 14 bit tag, indicating which queue memory bank (130, 131) a packet will be stored in (Rusu, col. 3, lines 35-37). Rusu further discloses that each internal cell as output by the input processors (101, 102) is assigned a queue number by the queue controller (140). The queue number is appended to the respective cells by the input processors (101, 102) and placed in a routing tag field within each cell (Rusu, col. 4, lines 11-16).

In Figure 5, Rusu further discloses that the queue controller (140) defines a memory location where the prepared cell will be sent based on the current queue memory bank (130, 131) availability, and if both banks (130, 131) are available, the bank chosen is that bank having the most available free memory space. If a memory bank (130 or 131) is currently in use, the queue controller (140) sends the prepared cell to the idle bank not in use. The dual bank queue memory system of Rusu allows for concurrent reading and writing to memory (Rusu, col. 4, lines 32-46).

The Office alleged that Rusu discloses "placing the determined address in an entry of a prior-determined address in the queue to form a linking list," citing Figure 5, box 365 – update link list for that queue, column 3, lines 38-39 and lines 51-53, and column 4, lines 55-57 (See Office Action at pages 2-3).

In the *Response to Arguments*, the Office further alleged that Rusu discloses the aforementioned features recited in claims 1, and similarly recited in claims 8, 9, 10, 16, and 17, citing column 3, lines 32-46.

Applicant respectfully disagrees with the Office's assertions that the aforementioned citations within the disclosure of Rusu disclose the features recited in claim 1, and similarly recited in claims 8, 9, 10, 16, and 17.

Rather, as previously noted, Rusu discloses appending the *queue number* in a routing tag field within each cell which is stored in an available queue memory bank (130, 131). Continuing with Figure 5, Rusu further discloses that data in the memory banks (130, 131) is maintained in the form of queues on a FIFO (first in, first out) basis,

organized by a link list (102) maintained by the queue controller (140) with the control memory (145) (Rusu, col. 4, lines 47-57). Rusu further discloses that the link list (102), maintained by the queue controller (140), organizes data stored in the available queue memory banks (130, 131). Hence, Rusu fails to disclose or suggest that the "queue number" is placed in an entry of a prior-determined address in the queue to form a linking list.

Further, Applicant respectfully submits that the Office's arguments presented in the *Response to Arguments* fail to demonstrate that the "queue number," which the Office Action referred to as the "determined address" (see page 2 of the Office Action, second bullet) is placed "in an entry of a prior-determined address in the queue for form a linking list" (emphasis added) as recited in the claims. As noted in the Office Action, a Multicast Mask, which is a 46 bit attachment, is attached to a packet for indicating that the packet can be transmitted or routed anywhere. The queue controller uses a two-stage Multicast Mask for selecting an output processor (160, 161) and for utilizing geographically distributed bits for geographically designating that a packet of interest is geographically limited as to transmission (Rusu, col. 3, lines 39-46). Rusu further discloses a Control Number, which is a 2-bit tag that indicates the start of a packet, end of a packet, and a normal cell in packet (Rusu, col. 3, lines 37-39). Rusu further discloses that data in the memory banks (130, 131) is maintained in the form of queues on a FIFO basis, organized by a link list (120) maintained by the queue controller (140) (See Figure 2); however, Rusu fails to discloses that the "queue number" is placed "in an entry of a prior-

determined address in the queue for form a linking list" (emphasis added) as recited in the claims.

Further, on page 2 of the Office Action, the Office refers to the "queue number" to allege that Rusu discloses the "determined address," and subsequently refers to the "Multicast Mask is a 46 bit attachment" to allege that Rusu discloses the "placing the *determined address* in an entry of a prior-determined address in the queue to form a linking list" (See Office Action on pages 2-3 – third bullet). Therefore, the Office improperly refers to two separate elements to improperly allege that Rusu discloses the aforementioned features recited in the claims.

Accordingly, Rusu fails to disclose or suggest every feature recited in claim 1. For similar reasons, Applicant respectfully submits that Rusu fails to disclose or suggest every feature recited in claims 8, 9, 10, 16, and 17.

Claims 2-7 depend from claim 1. Claims 11-15 depend from claim 10. Accordingly, claims 2-7 and 11-15 should be allowable for at least their dependency upon an allowable base claim, and for the specific limitations recited therein.

Therefore, Applicant respectfully requests withdrawal of the rejections of claims 1-17 under 35 U.S.C. §102(b), and respectfully submits that claims 1, 8, 9, 10, 16, and 17, and the claims that depend therefrom, are in condition for allowance.

CONCLUSION

In conclusion, Applicant respectfully submits that Rusu fails to disclose or suggest every claim feature recited in claims 1-17. The distinctions previously noted are more than sufficient to render the claimed invention unanticipated. It is therefore respectfully requested that all of claims 1-17 be allowed, and this present application be passed to issuance.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, Applicant's undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

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